RX14-17

Attachment 1 – Research Topic Template

1. **Research Title:** Strain Resilient Electronics: Materials and Process Development for Electronics Packaging Survivable in Highly Dynamic Environment

2. **Individual Sponsor:**

Dr. Ajit K Roy, AFRL/RXAN
AFRL/RXAN Bldg 654
2941 Hobson Way
WPAFB, OH 45433-7750
Ajit.roy@wpafb.af.mil

3. **Academic Area/Field and Education Level:** Materials Science and Engineering, Chemical Engineering, Mechanical Engineering, Electrical Engineering. (MS or Ph.D. level)

4. **Objectives:** To develop materials for highly transient strain and frequency tolerant electronic interconnects for flexible electronics packaging. Fundamentals of coupled electrical, mechanical and thermal properties of flexible electronic interconnects materials are to be studies through developing appropriate materials processing, testing and characterization. Nano constituents based innovative materials processing approaches and materials property optimization for printing of interconnects are to be pursued in connection with scale-appropriate materials modeling.

5. **Description:** Commercial off-the-shelf (COTS) electronics products are not designed to perform in extremely transient high impact scenarios. In many DoD high impact scenarios, the interconnect materials in electronics packaging undergoes through high strain rate (high-g), in which case severe degradation of the materials (electrical, mechanical, and thermal) properties along with the interconnect junctions failure, due to high strain gradient and high strain rate, dramatically limits the device performance. The survivability of electronics in such harsh environments is therefore a coupled multiphysics and multiscale materials development and design issue. Traditional interconnects material (e.g., solder) suffer from very limited performance life under high strain rate and gradient due to its relatively low durability and low strain-to-failure characteristics. Conductive nano constituents (carbon nano tubes, graphene, etc.) hybridizing with polymers or other high-strain alloys (the matrix phase), with appropriate network morphology and interface junction engineering between the nano constituents and the matrix, appears to show promise in bridging the materials conductivity (electrical and thermal) with strain resiliency. Atomistic scale material modeling has an important role to play in defining the materials interface morphology between the nano constituents and the matrix (polymer or other alloys) phase. Thin film deposition technology (plasma or physical vapor deposition, etc.) is useful in this regard for processing the suitable interface morphology. The goals of this research project will be to assess durability of the nano constituent junctions and its network morphology connectivity under high frequency fatigue and high strain gradient field. The key issues to be addressed are (1) robust nano constituent junction and nano constituent and matrix phase morphology design to ensure acceptable electrical/mechanical/thermal performance under high frequency fatigue, (2) bench mark the performance against the industry standard interconnect materials, and (3) correlation of material properties to device performance.

6. **Research Classification/Restrictions:** This research has no ITAR restrictions.

7. **Eligible Research Institutions:** Indicate to what organizations this topic should be provided.

■ DAGSI (Wright State University, AFIT, Ohio State University, University of Dayton, Miami University, Ohio University, University of Cincinnati)
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