RY15-1

1. **Research Title:** Investigation of Asynchronous Design Approaches for Wideband Digital Beamforming
2. **Individual Sponsor:** List the AFRL research topic sponsor's contact information

Mr. Peter E. Buxa, AFRL/RYDR
AFRL/RYDR Bldg 620
2241 Avionics Circle
WPAFB, OH 45433-7333
Peter.Buxa@wpafb.af.mil

3. **Academic Area/Field and Education Level:** Electrical/ Computer Engineering / Digital Signal Processing (BA/BS, MS, PhD level)
4. **Objectives:** Investigate the benefits of Asynchronous based processing as it relates to a wideband digital beamforming application. Research various Asynchronous architectures, design methodologies, and available hardware and quantify their performance, area, and power consumption over traditional clocked architectures such as those found with Xilinx or Altera based Field-Programmable Gate Arrays (FPGAs) or custom Application Specific Integrated Circuits (ASICs). Research may also include asynchronous programming within traditional FPGAs.
5. **Description:** The proposed project will investigate the benefits of asynchronous approaches as they relate to a wideband digital beamforming (>500 MHz instantaneous) application. Many wideband digital signal processing algorithms that are implemented within traditional FPGAs or ASICs and are designed to maximize throughput to match the high sampling rates of the Analog-to-Digital (A/D) or Digital-to-Analog (D/A) converters they interface with. In addition, wideband beamforming needs to account for frequency dependent response variations, so calibration and weighting operations are no longer simple complex multiplies. Hence, significantly more processing hardware is necessary. Many of these algorithms are feed-forward implementations that do not contain branches or loops more associated with general processing applications. Asynchronous logic is well-suited for feed-forward applications and may have benefits over traditional clocked approaches. This research intends to quantify the benefits of Asynchronous design in terms of design area, power, and performance (throughput and latency) using either asynchronous design techniques in traditional FPGA hardware or custom ASIC designs in advanced CMOS processes (65 nm or less). AFRL will assist with the beamforming algorithm and can provide sample code for signal processing on high sample rate data. Opportunities exist to use AFRL FPGA development boards as well as ASIC fabrication runs on an IBM CMOS process through the Trusted Access Program Office (TAPO).
6. **Research Classification/Restrictions:** This research has ITAR restrictions.
7. **Eligible Research Institutions:** Indicate to what organizations this topic should be provided
   - ✓ **DAGSI** (Wright State University, AFIT, Ohio State University, University of Dayton, Miami University, Ohio University, University of Cincinnati) NOTE: Topics submitted to DAGSI must be approved for public release. Need PA Approval #

☐ **AFIT** (only)

☐ **USAFA** (only)

If you are submitting a topic for the USAFA, indicate if you are also interested in sponsoring a USAF Cadet in summer 2015 (Average cost for USAF Cadet for 33 days is $5000)

☐ Yes ☐ No