1. **Research Title:** "Investigation of Asynchronous FPGA-Based Design Approaches for Wideband Digital Beamforming"

2. **Individual Sponsor:**

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3. **Academic Area/Field and Education Level:** Electrical/ Computer Engineering / Digital Signal Processing (BA/BS, MS level)

4. **Objectives:** Investigate the benefits of Asynchronous FPGA-based processing as it relates to a wideband digital beamforming application. Research various Asynchronous FPGA architectures, design methodologies, and available hardware and quantify their performance, size, and power consumption over traditional clocked architectures such as those found with Xilinx or Altera based FPGAs. Research may also include asynchronous programming within traditional FPGAs.

5. **Description:** The proposed project will investigate the benefits of asynchronous FPGA approaches as they relate to a wideband digital beamforming (>500 MHz instantaneous) application. Many wideband digital signal processing algorithms that are implemented within traditional FPGAs are designed to maximize throughput to match the high sampling rates of the Analog-to-Digital (A/D) or Digital-to-Analog (D/A) converters they interface with. In addition, wideband beamforming needs to account for frequency dependent response variations, so calibration and weighting operations are no longer simple complex multiplies. Hence, significantly more processing hardware is necessary. Many of these algorithms are feed-forward implementations that do not contain branches or loops more associated with general processing applications. Asynchronous FPGA logic is well-suited for feed-forward applications and may have benefits over traditional clocked approaches. This research intends to quantify the benefits of Asynchronous FPGA design in terms of design area, power, and performance (throughput and latency) using either asynchronous design techniques in traditional FPGA hardware or specially designed asynchronous digital technology (e.g. Achronix). AFRL will provide a design kit for the Achronix Scalar60 asynchronous FPGA that can be used for this research. In addition, AFRL will assist with the beamforming algorithm and can provide sample code for signal processing on high sample rate data.

6. **Research Classification/Restrictions:** This research has ITAR restrictions.

7. **Eligible Research Institutions:** Place an X in all that apply.

X Universities (DAGSI) ☐ AFIT (only) ☐ USAFA

8. **Interest in Summer USAFA Cadet (Avg Cost for USAF Cadet for 33 days was $5000):**

If you are submitting a topic for the USAFA, please indicate if you are also interested in sponsoring a USAF Cadet in summer of 2013